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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,840	12/09/2003	Hans M. Jacobson	YOR920030436US1 (8728-654	1311

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,840	JACOBSON ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *32-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31 and 38-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Paul Dinh

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the election filed on 1/6/06.

Claims 1-40 are pending.

Election/Restriction Requirement Issue.

The applicant states that simultaneous examination of pending claims will not present an undue burden on the Examiner.

The traverse and claims have been fully considered, and is not found persuasive because:

Due to different subject matter in the claimed groups, proper search and proper Examination of the entire application cannot be made without serious burden on the examiner.

The issue of serious burden on the examiner is one part of restriction requirements; the Other issue of restriction requirements that made the restriction required is because the application has 2 claimed groups that distinctly involve different subject matter.

Specifically group I drawn to invention with synthesis, without HDL and group II drawn to invention without synthesis, with HDL. Furthermore, group II recite elements such as compiler, technology mapper, optimizers, circuit generator that are not recited in group I.

Different subject matter requires searches in different areas.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Due to different subject matter in the claimed groups, proper search and proper examination of all groups cannot be made without serious burden on the examiner as proper search and proper examination requires searching in different subject areas.

Because these inventions are distinct for the reasons given above and the search required for one group is not required for other group(s), restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

The restriction requirement has been fully considered, fully reconsidered, **the requirement is still deemed proper and is therefore made FINAL.** The elected claims will be examined in this office action; the non-elected claims are withdrawn from consideration. The applicants are advised that cancellation of non-elected claims is required.

Claim Objections

Claims 19 and 40 are objected to because "invert" should be changed to "inverter".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 1-31 and 38-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 8, 29 and 38 are rejected because "leakage sensitivities" is not defined in the claims. Dependencies of claims 1, 8, 29 and 38 are rejected because they depend from claims 1, 8, 29 and 38.

Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form The basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –
(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-12, 16-19, 29-31, 38, 40 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Acar et al (US Pub. 2005/0044515)

(Claims 1, 8, 29, 38)

A memory device for storing a program (fig 13);

A processor in communication with the memory device (fig 13), the processor operative with the program to:

Receive a circuit model, wherein the circuit model has one or more circuit gates (one or more of fig 1, 6-7, 10-11);

Receive a library having one or more logic gates, wherein each logic gate has a topology *(fig 10)*

Calculate leakage sensitivities for each of the topologies (one or more of fig 1-7, 9-12); and

Synthesize (para 0031, 0051) a new circuit model by selecting one or more of the topologies based on its leakage sensitivities, wherein the new circuit model has reduced current leakage (one or more of: fig 4-5, 10-12, abstract, para 0003, 0006, 0008, 0032-0033, 0062).

(Claims 2, 9, and 30) wherein the processor is further operative with the program to: output the new circuit model (fig. 10, 13).

(Claims 3, 12) Wherein the leakage sensitivities are determined by a topology dependent leakage analytical model (one or more of: fig 6-13).

(Claim 4) wherein the leakage sensitivities are determined by measuring the leakage current of the logic gate in a circuit simulator while applying various input patterns to the logic gate (one or more of para 0008, 0041, 0051-0052, 0054, 0060-0067, fig 7, 9-12).

(Claims 5-7, 16-18, 31) wherein the processor is further operative with the program to: optimize current leakage of the new circuit model (fig 1-7, 9-12); optimize timing of the new circuit model (para 0008, 0062-0063); optimize area of the new circuit model (para 0002-0003).

(Claims 10-11) further comprising: receiving a probability model indicating the probability of one or more of the logic gates being in an input state (fig 6, 9-11); indicating the probability of one or more transistors being in an input state (fig 6, 9-11).

(Claims 19, 40) wherein the logic gates are selected from the group consisting of: and, or, nand, nor, xor, and invert (fig 6)

2. Claims 1-12, 15-19, 29-31, 38-40 are rejected under 35 U.S.C. 102(b) as being anticipated by the prior art of record Usami et al (US Pub. 2002/0144223)

(Claims 1, 8, 29, 38)

A memory device for storing a program (fig 1, 6, 11);

A processor in communication with the memory device (fig 1, 6, 11), the processor operative with the program to:

Receive a circuit model, wherein the circuit model has one or more circuit gates (one or more of fig 1-2, 5-10, 12-14);

Receive a library having one or more logic gates, wherein each logic gate has a topology (*one or more of: 1-2, 6-14*)

Calculate leakage sensitivities for each of the topologies (one or more of fig 1, 3-14); and

Synthesize a new circuit model by selecting one or more of the topologies based on its leakage sensitivities, wherein the new circuit model has reduced current leakage (one or more of fig 1, 3, 5-7, 11-14).

(Claims 2, 9, and 30) wherein the processor is further operative with the program to: output the new circuit model (one or more of fig. 1, 3, 5-7, 11-14).

(Claims 3, 12) Wherein the leakage sensitivities are determined by a topology dependent leakage analytical model (one or more of: fig 1, 3, 5-7, 11-14).

(Claim 4) wherein the leakage sensitivities are determined by measuring the leakage current of the logic gate in a circuit simulator while applying various input patterns to the logic gate (one or more of para 0042, 0047, 0049, 0073, fig 1, 3-7, 9-10).

(Claims 5-7, 16-18, 31) wherein the processor is further operative with the program to: optimize current leakage of the new circuit model (fig 3, 5-7, 11-14); optimize timing of the new circuit model (fig 3, 5-7, 11-14); optimize area of the new circuit model (fig 3, 5-7, 11-14).

(Claims 10-11) further comprising: receiving a probability model indicating the probability of one or more of the logic gates being in an input state (para 0078); indicating the probability of one or more transistors being in an input state (para 0078).

(Claim 15) wherein the synthesizing step further comprises: substituting one or more logic gates from the circuit model to create the new circuit model (one or more of: fig 1, 3, 5, 7, 11-14).

(Claims 19, 40) wherein the logic gates are selected from the group consisting of: and, or, nand, nor, xor, and invert (one or more of fig 2, 8, 10)

(Claim 39) wherein the optimization algorithm is selected from the group consisting of: kernel factoring, decomposition, technology mapping and buffering (one or more of: 6-7, 11-13)

3. Claims 1-19, 29-31, and 38-40 are rejected under 35 U.S.C. 102(b) as being anticipated by the prior art of record Khouja et al (USP 6345379)

(Claims 1, 8, 29, 38)

A memory device for storing a program (fig 2A);

A processor in communication with the memory device (Fig 2A), the processor operative with the program to:

Receive a circuit model, wherein the circuit model has one or more circuit gates (one or more of fig 1, 2B, 3, 6, 10-12, 14-21);

Receive a library having one or more logic gates, wherein each logic gate has a topology (*one or more of: abstract, fig 1, 10-11, col 10 line 50, col 11 lines 4, 32, col 12 line 50+, col 48, 50*)

Calculate leakage sensitivities for each of the topologies

(*See the following rejections of one or more of claims 3-4, 12 for leakage sensitivities and/or leakage sensitivity are one or more of: sensitization in fig 4, power dissipation modeling of component (col 4 line 66), static/dynamic power dissipation, net switching power dissipation (col 4), leakage models/calculations in col 49-59, leakage power estimation (col 10)*); and

Synthesize a new circuit model by selecting one or more of the topologies based on its leakage sensitivities, wherein the new circuit model has reduced current leakage (*one or more of: col 12 line 50+, col 48, 50, fig 3-5, 19-20*).

(Claims 2, 9, 30) wherein the processor (fig 2A) is further operative with the program to: output the new circuit model.

(Claims 3, 12) wherein the leakage sensitivities are determined by a topology dependent leakage analytical model (one or more of: fig 3-5, col 47-48, 50-58).

(Claim 4) wherein the leakage sensitivities are determined by measuring the leakage current of the logic gate in a circuit simulator while applying various input patterns to the logic gate (one or more of col 13, col 17 line 62+, col 48).

(Claims 5-7, 16-18, 31) wherein the processor is further operative with the program to: optimize current leakage of the new circuit model (fig 2-5, col 48-58); optimize timing of the new circuit model (fig 2-5, col 48-58); optimize area of the new circuit model (fig 2-5, col 48-58).

(Claims 10-11) further comprising: receiving a probability model indicating the probability of one or more of the logic gates being in an input state (one or more of fig 4-5, summary, col 18-21, 47); indicating the probability of one or more transistors being in an input state (one or more of fig 4-5, summary, col 18-21, 47).

(Claims 13, 14, 15) wherein the synthesizing step further comprises: adding one or more logic gates to the circuit model to create the new circuit model (col 7 lines 42-45); deleting one or more logic gates from the circuit model to create the new circuit model (col 22 line 12+); substituting one or more logic gates from the circuit model to create the new circuit model (one or more of: fig 19-20, col 22 line 6).

(Claims 19, 40) wherein the logic gates are selected from the group consisting of: and, or, nand, nor, xor, and invert (one or more of fig 2, 6, 10-12, 14-21, 25)

(Claim 39) wherein the optimization algorithm is selected from the group consisting of: kernel factoring, decomposition, technology mapping and buffering (one or more of: fig 1, 3, 5, col 5 line 3, col 42 line 25)

Allowable Subject Matter

Claims 20-28 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 20-28 would be allowable because the prior art of record does not teach or suggest the limitation in claim 20.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Primary Examiner